LATERAL SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a lateral semiconductor device formed on an SOI substrate and a method for producing the same.

[0003] 2. Prior Art

[0004] In recent years, products, each comprising high withstand voltage lateral semiconductor devices formed on a silicon-on-insulator (SOI) substrate and low withstand voltage circuits and being integrated on a single chip, have been developed for use in color PDPs.

[0005] For the purpose of reducing the area of a high withstand voltage lateral MOS transistor device, it is necessary to improve its current capabilities (ON-resistance and drain saturation current) while maintaining its target withstand voltage.

[0006] In addition, it has become important to raise the on-state breakdown voltage of the device, that is, to improve the safe operation area (SOA), and to improve the ESD resistance of the device. Furthermore, the structure of the device has been studied (Patent Publication No. 3473460 and Tokuhyo No. 2000-505955). For example, raising impurity concentration in the region between the source region and the buried insulating film of a device, described in Japanese Laid-open Patent Application No. 2000-216393, has been proposed as a method for the improvement. **FIG. 11** is a sectional view showing the structure of the device.

[0007] An N-type semiconductor layer **3** is bonded onto a support substrate **1** isolated by a buried insulating film **2**. In the N-type semiconductor layer **3**, a P-well region **5**, an N^+-source region **6**, an N^+-drain region **4** and a P^+-contact diffusion region **7** are diffused. Above the P-well region **5**, a gate electrode **9** is formed on a gate insulating film **8** and extended to the upper side of a field oxide film **13**. A P-type buried region **12** having a low resistance is inserted between the N^+-source region **6** and the buried insulating film **2**. On the N^+-source region **6** and the P^+-contact diffusion region **7**, a source electrode **10** is formed, and on the N^+-drain region **4**, a drain electrode **11** is formed.

[0008] When the device is on-state and as its drain voltage is raised, the device is saturated and its drain current becomes constant. When the drain voltage is raised further, avalanche breakdown occurs on the drain side owing to the Kirk effect. The hole current thus generated flows to the P-type buried region **12** directly under the N^+-source region **6**. This current causes a voltage drop directly under the N^+-source region **6**, and the voltage of the P-type buried region **12** rises. When the voltage rises higher than the source voltage and becomes the built-in potential or more, the turn-on of a parasitic bipolar transistor comprising the N^+-source region **6**, the P-type buried region **12** and the N^+-drain region **4** is occurred. At the turn-on of parasitic bipolar transistor, the snap-back phenomenon occurs, large current flows, thereby causing breakdown. Hence, for the purpose of raising the breakdown voltage and expanding the SOA, it is important to suppress the turn-on of the parasitic bipolar transistor and the Kirk effect.

[0009] Since the P-type buried region **12** having high impurity concentration is inserted between the N^+-source region **6** and the embedded insulating film **2**, the parasitic resistance under the N^+-source region **6** is reduced, and a voltage drop is also reduced. With this configuration, the voltage at the turn-on of the parasitic bipolar transistor can be raised, and the SOA can be improved.

[0010] The device structure disclosed in Japanese Laid-open Patent Application No. 2000-216393, the prior art, has two problems described below.

[0011] A first problem is that, when the withstand voltage of an NMOS transistor in particular is raised to 100 V or more, its on-state breakdown voltage is insufficient.

[0012] In the case that the impurity concentration in the P-well region is low, when the drain voltage is raised, the expansion of the depletion region to the P-well region increases. Hence, if the interval between the N^+-source region and the N-type semiconductor layer (drift region) is small, the depletion region reaches the N^+-source region, and punch-through occurs, and the off-state breakdown voltage lowers. Furthermore, with respect to the on-state breakdown voltage, the depletion region expands to the P-well region, and Vth is apt to lower owing to the short channel effect. As a result, the drain saturation current increases, and the on-state breakdown voltage lowers.

[0013] On the other hand, in the case that the impurity concentration in the P-well region is high, Vth rises, the ON-resistance increases, and the drain saturation current lowers. As a result, the on-state breakdown voltage is raised. However, since the current capabilities are lowered, the area of the device increases.

[0014] A second problem occurs in the case of a PMOS transistor in particular.

[0015] For the purpose of suppressing the turn-on of the parasitic bipolar transistor to raise the on-state breakdown voltage, it is effective to reduce the parasitic resistance by raising the impurity concentration in the buried layer.

[0016] As practical production methods for forming a buried layer having high impurity concentration, two methods are available: the high-energy ion implantation method and the epitaxial growth method.

[0017] However, since the buried region of the PMOS transistor is an N-type, there are three kinds of impurities: phosphorus, arsenic and antimony. In comparison with the range Rp of boron in an NMOS transistor, the ranges Rp of these impurities are small. If ion implantation is carried out under a high-dose condition, ion implantation time per wafer becomes long, and productivity is lowered. Hence, in reality, it is frequently difficult to carry out high-dose ion implantation.

[0018] For this reason, in the case of the PMOS transistor, a production means for easily forming a buried layer having high impurity concentration is to bury a diffusion layer using epitaxial growth.

[0019] However, since the buried diffusion layer is formed first by diffusion processing, its heat treatment time becomes long in comparison with the heat treatment time for the other diffusion layers. Hence, if a buried layer having high impurity concentration is formed under the gate electrode to